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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,628	07/15/2003	John Xiaoxiong Zhong	4162P001C	1718

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,628	ZHONG ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-12,14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-12,14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

1. Claims 1-4, 6-14, and 16-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1—2, 4, 6-7, 11-14, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by York, G., et al., "An Integral environment for HDL Verification" (hereinafter referred to as York).

3. York was cited in a prior office action dated 7/30/02.

4. As for claim 1, York disclosed the invention as claimed, including a method for performing design verification [pg. 9, abstract], the method comprising:

specifying at least one hardware description language object that represents at lest one signal as a symbol in a design using a first statement that is part of a description language [pg. 12, section 3.1; pg. 14, section 3.3, pg. 12, fig. 2, module alu, output, where mode is symbolic expression, pg. 13, fig. 3, and pg. 14, section 3.3 fourth paragraph where the UART of fig. 3 is shown to inputs set to symbolic expressions: Note that the statements of the module description are part of "a description language"]; and

instructing a symbolic simulator in response to the first statement to treat the at least one description language object as a symbol [pg. 14, section 3.3, where the response to the description language objects, (the modules described in fig.'s 2 and 3) are symbolically simulated].

5. As for claim 11, York disclosed the invention as claimed, including an article of manufacture having at least one recordable medium having stored thereon executable instruction which, when executed by at least one processing device cause the at least one processing device to::

specify at least one hardware description language object that represents at lest one signal as a symbol in a design using a first statement that is part of a description language [pg. 12, section 3.1; pg. 14, section 3.3, pg. 12, fig. 2, module alu, output, where mode is symbolic expression, pg. 13, fig. 3, and pg. 14, section 3.3 fourth paragraph where the UART of fig. 3 is shown to inputs set to symbolic expressions: Note that the statements of the module description are part of "a description language"]; and

instructing a symbolic simulator in response to the first statement to treat the at least one description language object as a symbol [pg. 14, section 3.3, where the response to the description language objects, (the modules described in fig.'s 2 and 3) are symbolically simulated. Also note that York inherently disclosed and article of manufacture having at least one recordable medium having stored thereon executable instruction because the a computer program product having instruction which must be stored on a computer readable medium and be executed by a processing device in order to perform the functions of the function of verification as disclosed by York.].

6. As for claims 2, 4, 6, 12-14 and 16, York further disclosed
[claims 2 and 12] inserting the first statement into a design specification [fig. 2, see input, mode] and inputting the design specification into the symbolic simulator [pg. 14,

section 3.3, first paragraph, lines 1-3, and paragraph four, lines 1-3, where the input is utilized by the symbolic simulator];
[claims 4 and 14] wherein the at least one description language object comprises a Verilog object [fig. 2];
[claims 6 and 16] wherein the at least one signal comprises an input [fig. 2, see input, mode];
[claims 7 and 17] specifying a check using a second statement, the check to perform a test to validate design functionality; and instructing the symbolic simulator using the second statement to perform the test [pg. 14, section 3.3, fourth paragraph: Note that the examiner interprets the use of the symbolic simulator to perform a check/test for verification to inherently include at least a statement that causes the simulator to do the checking, and therefore reads on a second statement as claimed]. HDL, Verilog, PLI [pg. 98, right hand side, lines 1-14, and also as cited in the rejection of claim 1].

7. As for claims 8 and 18, York further disclosed inserting the first and second statements into a design specification and instructing the symbolic simulator using the second statement to perform the test [see fig.'s 2 and 3, out and case, which signify the simulation with outputs to the variables out and state_reg, respectively; and pg. 14, section 3.3, especially 14, section 3.3, first paragraph, lines 1-3, and paragraph four, lines 1-3, where the input is utilized by the symbolic simulator].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-10, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over York, G., et al., "An Integral environment for HDL Verification" (hereinafter referred to as York), in view of Dawson, Charles, et al., "The Verilog Procedural Interface for the Verilog hardware description language".

9. As for claims 9 and 19, York in view of Dawson disclose the invention substantially as claimed, including the method and apparatus for performing design verification as cited in the rejections of claims 1, 11, and 7-17.

York does not disclose that the second statement comprises a PLI.

Dawson discloses a PLI statement [pg. 17, PLI, pg. 18, left hand side, first full paragraph, pg. 21-22, section 4.2, the declaration of wire]. Dawson further discloses that the specifying the hardware declaration language object through the use of the first statement (VPI creation of the object) would be desirable [pg. 22, section 4.4 first paragraph].
Dawson discloses a second statement that is a PLI command [pg. 21, section 3.2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of York and Dawson because having Dawson's second statement comprised of a PLI command would have improved York's system by requiring very little user interaction by automatically executing the simulation [see Dawson, pg. 21, section 3.2].

10. As for claims 10 and 20, York in view of Dawson discloses the invention substantially as claimed, including the method and apparatus for performing design verification as cited in the rejections of claims 1, 11, and 7-17.

York does not specifically disclose instructing the symbolic simulator to generate a file with information to locate an identified fault.

Dawson discloses instructing the symbolic simulator to generate a file with information to locate an identified fault [pg. 20, section 2.7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of York and Dawson because having Dawson's symbolic simulator instructed to generate a file with information to locate an identified fault would have improved York's system by complementing the rest of the interface with the added ability to write files which provide valuable error information that could be useful to a designer for finding errors.

11. Applicant's arguments filed September 19, 2005 have been fully considered but they are not persuasive.

In the remarks, applicant argues in substance:

A: York or the combination of York and Dawson do not disclose specifying at least one hardware description language object that represents at lest one signal as a symbol in a design

Examiner respectfully disagrees for the following reasons:

As to A: York discloses specifying at least one hardware description language object that represents at lest one signal as a symbol in a design [pg. 12,

section 3.1; pg. 14, section 3.3, pg. 12, fig. 2, module alu, output, where mode is symbolic expression, pg. 13, fig. 3, and pg. 14, section 3.3 fourth paragraph where the UART of fig. 3 is shown to inputs set to symbolic expressions: Note that the statements of the module description are part of "a description language". Further, York disclose at page 14, section 3.3, 1st to 4th paragraphs that the fig. 3 example, the UART (described in a hardware description language) symbolic simulation is done on the inputs (signals) and that using the input signals in this way is using the input as a symbol].

12. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
December 12, 2005